APPLICATION NO. 10/033785

October 4, 2005

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CLMPTO

1. (Currently Amended) A microelectronic device, comprising:

a substrate;

a ~~non-composite~~ single semi-insulating silicon carbide layer formed on the substrate, the semi-insulating silicon carbide layer comprising boron and a shallow donor impurity, the semi-insulating silicon carbide layer having boron-related D-center defects formed therein; and

a first semiconductor device formed on the semi-insulating silicon carbide layer, the first semi-conductor device having an active area comprising a high bandgap material.

2. (Original) The device of Claim 1, wherein the semi-insulating silicon carbide layer is formed epitaxially.

3-4. (Canceled)

5. (Previously Presented) The device of Claim 2, wherein the first semiconductor device is a high frequency device.

6. (Previously Presented) The device of Claim 2, wherein the first semiconductor device is a high power device.

7. (Original) The device of Claim 1, wherein the substrate is a conductor.

8. (Original) The device of Claim 1, wherein the substrate comprises n^+ silicon carbide.

9. (Original) The device of Claim 1, wherein the semi-insulating silicon carbide layer comprises 6H silicon carbide.

10. (Original) The device of Claim 1, wherein the semi-insulating silicon carbide layer comprises 4H silicon carbide.

11. (Previously Presented) The device of Claim 1, wherein the active area of the first semiconductor device comprises silicon carbide.

12. (Original) The device of Claim 1, wherein the first semiconductor device comprises a metal-oxide-semiconductor field effect transistor.

13. (Previously Presented) The device of Claim 1, wherein the first semiconductor device comprises a lateral metal-oxide-semiconductor field effect transistor.

14. (Original) The device of Claim 1, wherein the first semiconductor device comprises a bipolar junction transistor.

15. (Original) The device of Claim 1, wherein the first semiconductor device comprises a junction field effect transistor.

16. (Original) The device of Claim 1, further comprising:

at least a second semiconductor device.

17. (Original) The device of Claim 16, wherein the at least a second semiconductor device is found on a portion of the substrate that is physically isolated from the first semiconductor device.

18. (Original) The device of Claim 16, wherein the at least a second semiconductor device is found on a portion of the substrate that is electrically isolated from the first semiconductor device.

19. (Previously Presented) The device of Claim 1, wherein the first semiconductor device is formed epitaxially.

CLAIMS 20-37 (CANCELLED)

38. (Currently Amended) An integrated circuit device comprising:

a conducting substrate;

a first ~~non-composite~~ single semi-insulating silicon carbide layer formed over a first portion of the conducting substrate, the first ~~non-composite~~ single semi-insulating silicon carbide layer ~~being doped with~~ comprising boron and a shallow donor impurity, the ~~non-composite~~ first single semi-insulating silicon carbide layer having boron-related D-center defects formed therein;

a first device formed over at least part of the first portion of the substrate; and

a second device formed over a second portion of the substrate different from the first portion,

wherein the ~~first non-composite semi-insulating silicon carbide layer electrically insulates the~~ first device is electrically isolated from the second device.

39. (Currently Amended) The integrated circuit device of Claim 38, wherein the first device is formed over at least part of the first semi-insulating silicon carbide layer.

40. (Previously Presented) The integrated circuit device of Claim 38, wherein the first device is a high power device.

41. (Previously Presented) The integrated circuit device of Claim 40, wherein the second device is a control device.

42. (Previously Presented) The integrated circuit device of Claim 38, wherein the first device is a high frequency device.

43. (Previously Presented) The integrated circuit device of Claim 42, wherein the second device is a control device.

44. (Previously Presented) The integrated circuit device of Claim 39, wherein the first device is a lateral device.

45. (Previously Presented) The integrated circuit device of Claim 39, wherein the second device is a control device.

46. (Previously Presented) The integrated circuit device of Claim 39, wherein the second device is a vertical device.

47 - 48. (Canceled).

49. (Previously Presented) The microelectronic device of Claim 1, wherein the shallow donor impurity is nitrogen.

50. (Previously Presented) The microelectronic device of Claim 1, wherein the semi-insulating silicon carbide layer is formed by epitaxial growth.

51. (Currently Amended) The microelectronic device of Claim 50, wherein the shallow donor impurity is nitrogen, and wherein the semi-insulating silicon carbide layer is co-doped with boron and nitrogen during epitaxial growth.

52. (Previously Presented) The integrated circuit device of Claim 38, wherein the shallow donor impurity is nitrogen.

53. (Previously Presented) The integrated circuit device of Claim 38, wherein the semi-insulating silicon carbide layer is formed by epitaxial growth.

54. (Currently Amended) The integrated circuit device of Claim 53, wherein the shallow donor impurity is nitrogen, and wherein the semi-insulating silicon carbide layer is co-doped with boron and nitrogen during epitaxial growth.

55. (New) The integrated circuit device of Claim 46, further comprising a second single semi-insulating silicon carbide layer comprising boron and a shallow donor impurity, the second single semi-insulating silicon carbide layer having boron-related D-center defects formed therein;

wherein the second single semi-insulating silicon carbide layer is formed between the vertical device and the second portion of the conducting substrate, and is electrically isolated from the first semi-insulating silicon carbide layer.

56. (New) The integrated circuit device of Claim 38, further comprising a second single semi-insulating silicon carbide layer comprising boron and a shallow donor impurity, the second single semi-insulating silicon carbide layer having boron-related D-center defects formed therein;

wherein the second single semi-insulating silicon carbide layer is formed between the second device and the second portion of the conducting substrate and is electrically isolated from the first semi-insulating silicon carbide layer.